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VECTOR	131350
VECTORS	87226
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DB=PGPB; PLUR=YES; OP=OR			
L41	(interconnect and DRAM and chip and scalar and vector).clm.	0	L41
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L40	L39 and l1	18	L40
L39	(sushma or bratt or benkual or iwamoto or vaughn).in.	25306	L39
DB=PGPB; PLUR=YES; OP=OR			
L38	(sushma or bratt or benkual or iwamoto or vaughn).in.	1145	L38
L37	(interconnect and DRAM and controller$1 and chip and scalar and vector).clm.	0	L37
L36	((ic or integrated) and coheren$5 and DRAM and controller$1 and chip and scalar and vector).clm.	0	L36
L35	((ic or integrarted) and coheren$5 and DRAM and controller$1 and chip and scalar and vector).clm.	0	L35
L34	L33	0	L34
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L33	((ic or integrarted) and coheren$5 and DRAM and I near1 O near3 controller$1 and chip and scalar and vector).clm.	0	L33
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L32	L28 and l15	2	L32
L31	L28 and l14	3	L31
L30	L28 and l13	19	L30
L29	L28 and l12	29	L29
L28	l5 and (host$3 or DRAM or ram)	74	L28
DB=PGPB,USPT; PLUR=YES; OP=OR			
L27	l10 and l15	0	L27
L26	l10 and l14	1	L26
L25	l10 and l13	62	L25
L24	l10 and l12	121	L24
L23	l9 and l15	1	L23
L22	l9 and l14	1	L22
L21	l9 and l13	26	L21
L20	l9 and l12	41	L20
L19	l5 and l15	2	L19
L18	l5 and l14	3	L18
L17	l5 and l13	19	L17
L16	l5 and l12	36	L16
L15	(716/2-18)![CCLS]	10216	L15
L14	(710/305-317)![CCLS]	5688	L14
L13	(712/3-38, 225-228)[CCLS]	4772	L13
L12	(712/2-300)[CCLS]	13531	L12
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L11	l4 and l3	330	L11

L10	l1 and l3	367	L10
L9	L7 and l1	118	L9
L8	L7 and l5	17	L8
L7	vector$1 near7 permut$7	911	L7
L6	L5 and l3	18	L6
L5	L4 and l1	94	L5
L4	(south or north) near45 (bridge or interconnect$4 or crossbar$1 or switch$3 or gate$1 or rout$4)	15523	L4
L3	coheren$4 near15 (memor$4 or stor$4 or cach$4)	15446	L3
L2	coheran$4 near15 (memor$4 or stor$4 or cach$4)	7	L2
L1	(chip or chipset or interconnect$3 or ic) and (vector) and scalar	7016	L1

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1. **A236 parallel DSP chip provides real-time video processing economically and efficiently**
   Morton, S.G.;
   ELECTRO '96. Professional Program. Proceedings.
   30 April-2 May 1996 Page(s):261 - 268
   Digital Object Identifier 10.1109/ELECTR.1996.501237
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2. **Video DSP architecture for MPEG2 codec**
   Araki, T.; Toyokura, M.; Akiyama, T.; Takeno, H.; Wilson, B.; Aono, K.;
   Acoustics, Speech, and Signal Processing, 1994. ICASSP-94., 1994 IEEE International Conferenc
   Volume ii, 19-22 April 1994 Page(s):II/417 - II/420 vol.2
   Digital Object Identifier 10.1109/ICASSP.1994.389632
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